

What Is Claimed Is:

1           1. A gate for preventing dopants from penetrating a gate  
2 insulator, comprising:  
3           a gate insulator disposed on a substrate;  
4           a polysilicon layer disposed on the gate insulator; and  
5           an amorphous-silicon layer disposed on the polysilicon  
6 layer, wherein the gate is composed of the polysilicon layer and  
7 the amorphous-silicon layer.

1           2. The gate as claimed in claim 1, wherein the gate insulator  
2 is a gate oxide layer.

1           3. The gate as claimed in claim 1, wherein the thickness of  
2 the polysilicon layer is 300~1000Å.

1           4. The gate as claimed in claim 3, wherein the thickness of  
2 the amorphous-silicon layer is 1000~2000Å.

1           5. A method of forming a gate for preventing dopants from  
2 penetrating a gate insulator, comprising:  
3           providing a substrate;  
4           forming a gate insulator on the substrate;  
5           forming a polysilicon layer on the gate insulator;  
6           forming an amorphous-silicon layer on the polysilicon  
7 layer; and  
8           patterning the polysilicon layer and the amorphous-silicon  
9 layer to form a gate.

1           6. The method as claimed in claim 5, wherein the gate  
2 insulator is a gate oxide layer.

1           7. The method as claimed in claim 5, wherein the thickness  
2 of the polysilicon layer is 300~1000Å.

1           8. The method as claimed in claim 7, wherein the method of  
2 forming the polysilicon layer comprises using silane as a  
3 processing gas to deposit the polysilicon layer under 0.15~0.25  
4 torr at 580~630°C.

1           9. The method as claimed in claim 5, wherein the thickness  
2 of the amorphous-silicon layer is 1000~2000Å.

1           10. The method as claimed in claim 9, wherein the method of  
2 forming the amorphous-silicon layer comprises using silane as  
3 a processing gas to deposit the amorphous-silicon layer under  
4 0.15~0.25 torr at 510~560°C.

1           11. The method as claimed in claim 5, wherein after the step  
2 of patterning the polysilicon layer and the amorphous-silicon  
3 layer to form the gate, a source/drain is formed in the substrate  
4 beside the gate by ion implantation.

1           12. The method as claimed in claim 11, wherein after  
2 performing the ion implanting, an anneal process is performed.

1           13. The method as claimed in claim 11, wherein a dopant used  
2 in the ion implanting process is boron ions.

1           14. The method as claimed in claim 13, wherein in the  
2           implantation of boron ions, the dosage is  $1 \times 10^{15} \sim 1 \times 10^{16} \text{ cm}^{-2}$  and  
3           the implant energy is 3~20 keV.

1           15. The method as claimed in claim 11, wherein a dopant used  
2           in the ion implanting process is As ions.

1           16. The method as claimed in claim 15, wherein in the  
2           implantation of As ions, the dosage is  $1 \times 10^{15} \sim 1 \times 10^{16} \text{ cm}^{-2}$  and the  
3           implant energy is 30~80 keV.